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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 08/530,661
Filing Date: September 20, 1995
Appellant(s): KEETH ET AL.

Kevin Johanson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 14 July 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement of which claims stand or fall together is accepted.*(8)*

Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,838,038	Takashima et al.	11-1998
5,610,418	Eimore	3-1997

5,654,577	Nakamura et al.	8-1997
5,287,000	Takahashi et al.	2-1994

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 6 – 10, 18, 19, 22, 23, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashima et al. ('038) in view of Eimore, Nakamura et al. and Takahashi et al. ('000).

3. With respect to claim 6, Takashima et al. ('038) shows (see cover Figure and column 8, line 17 et seq.) a DRAM device where the cell size is $6F^2$ (column 25, line 17) but does not show the minimum feature size, peripheral circuitry, array size or packaging. Eimore shows (see cover figure and column 8, line 9) a DRAM (column 1, line 9) where a 0.25 micron design rule is used (column 10, line 61). Nakamura et al. shows a DRAM (see cover Figure and column 3, line 66 et seq.) where a 16 M device is shown (column 4, line 25) and shows the chip includes, besides the memory array, timing, address, redundancy, data, test path and voltage supply circuitry. Takahashi et al. ('000) show (see Figure 1 and column 5, line 67 et seq.) a DRAM (column 6, line 10) where the die is encapsulated in a package with pins extending outwardly. It would have been obvious to include the peripheral circuitry show by Nakamura et al. since it provides a

working device, to include the feature size shown by Eimore since it is known to be functional and to provide a 16M device since it is known to be useful. Note that with the 0.25 micron design rule the area of the memory is less than 6 mm^2.

4. With respect to claim 7, the memory array is shown by Takashima et al. ('038) as 4-level (see Figure 29 and column 26, line 34 et seq.) and since the peripheral circuitry does not have an integrated capacitor, it would inherently have less than 4-levels.

5. With respect to claim 8, Nakamura et al. show that Figure 1 matches the geometric arrangement of the actual chip and with the memory area being less than 6 mm^2, the whole chip will obviously be less than 35 mm^2.

6. With respect to claim 9, Takashima et al. ('038) shows a structure with 5-levels (see Figure 47 and column 28, line 63 et seq.) and since the peripheral circuitry does not have an integrated capacitor, it would inherently have less than 5-levels. Also the memory will have an area of less than 6 mm^2.

7. With respect to claim 10, Nakamura et al. show that Figure 1 matches the geometric arrangement of the actual chip and with the memory area being less than 6 mm^2, the whole chip will obviously be less than 35 mm^2 and Takashima et al. ('038) shows a structure with 5-levels (see Figure 47 and column 28, line 63 et seq.) and since the peripheral circuitry does not have an integrated capacitor, it would inherently have less than 5-levels. Also the memory will have an area of less than 6 mm^2.

8. With respect to claims 18, 19 and 25, the memory arrays with the density shown will have 270 devices in 100 $micron^2$.

9. With respect to claims 22, 23 and 26, the 16M device has no more than 68M memory cells and with the density shown will have 270 devices in 100 micron^2.

(11) Response to Argument

Appellant states (page 9, top) that the term design rule is misunderstood and that the design rule refers to a minimum dimension, but that is what Takashima et al.('038) refer to. Appellant then states that a device will include other features but doesn't say what other features. But note that Takashima et al. ('038) show the device size is $6F^2$ and not , $6F^2$ plus something else. Appellant then states that Eimore shows multiple dimensions and references Figure 6 and 9. First, note that Eimore is used to show the feature size, not the device design and Takashima et al. ('038) is relied upon the show the device size of $6F^2$. Second, the structure shown by Eimore in Figure 6, for instance, shows a size of 0.6 x 0.95 = 0.48 micron^2 (compare this to 0.375 micron^2 for the Takashima et al. ('038) case) and even that dimension will yield more than 16,000,000 cells. Thus Takashima et al. ('038) as modified by Eimore shows at least the claimed density of cells and even in the case where Eimore is improperly applied to the claim, it still shows a higher density.

Appellant then states (page 9, mid page) that some of the cells might be defective and to get the claimed cell density of working cells, that more than the 16M cells would be needed. First, no such margin is claimed and cannot be responded to. Also since it is unknown what factor would have to be applied, it cannot be responded to. Also note that Takashima et al. ('038) as modified by Eimore provides more than a factor of 2 greater density (i.e. the area is 6 vs 14 mm^2). This would seem to provide a large margin for error.

Appellant then states (page 10, top) that the claims are allowable since the invention is highly sought after. This is not a technical argument but note that the claimed invention is shown by the prior art.

Appellants further argues that there are problems inherent in shrinking the device size (page 10, bottom) but Takashima et al. ('038) show that it can be done and Eimore shows that a small feature size can be achieved. This shows that the claimed invention was within the state of the art at the time of the invention.

Appellant states (page 12, middle) that the dependent claims are allowable since the independent claims are allowable but as noted above the independent claims are not allowable and the dependent claims are similarly not allowable (see the rejection above).

With respect to claim 22 and the dependent claims, Appellant states that the combination of the references is in error (page 13, top) stating that the references do not show a device with no more than 68,000,000 cells. But note that the claim states that the number of cells is not more than 68,000,000 or put another way, it is less than or equal to 68,000,000. Certainly, 16,000,000 is less than 68,000,000. It is not known if this is an error in composing the claim but the claim was evaluated as written. It is worth noting, parenthetically, that Takashima et al. ('038) shows that DRAMs can be as large as 256 Mb (column 2, line 61) and therefore even the unclaimed cell number of 68,000,000 was known in the art at the time of the invention.

Appellant states (page 13, bottom) that claim 22 is allowable for the same reason that 6 and 18 are allowable and that more than the desired number of functional cells must be fabricated. This means that some of the cells might be defective and to get the claimed cell density of working cells, that more than the 16M cells would be needed. First, no such margin is

claimed and cannot be responded to. Also since it is unknown what factor would have to be applied, it cannot be responded to. Also note that Takashima et al. ('038) as modified by Eimore provides more than a factor of 2 greater density (i.e. the area is 6 vs 14 mm^2) Thus the argument appears to be moot.

Appellant states (page 14, middle) that the dependent claims are allowable since the independent claims are allowable but as noted above the independent claims are not allowable and the dependent claims are similarly not allowable (see the rejection above).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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July 28, 2004

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